AK

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,385	08/29/2000	Sanjay Dabral	042390.P5258D	9681

7590 11/06/2003

Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard Seventh Floor
Los Angeles, CA 90025

EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,385	DABRAL ET AL.	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-29* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. In view of the appeal brief filed on August 15, 2003, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 112

2. Claims 20-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. With regards to claim 20, it is unclear to the examiner whether the performance circuit and the protection circuit are formed on the same "integrated circuit substrate. Please note that claim 20 recited the use of different

substrates, e.g. "**an** integrated circuit substrate" [emphasis added], for each circuit (e.g. performance and protection circuit).

4. Claims 21-29 are rejected due to their dependency on claim 20.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 20-24 and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Roy (US Pat. No. 5,159,518).

Regarding claim 20, Roy teaches a method comprising the step of forming a performance circuit (130) occupying a first well of an IC substrate (120) (see fig. 7); forming a protection circuit (104, 102) occupying a second well of an IC substrate (120) separate from the first well (see fig. 7); and coupling the protection circuit (104, 102) to the performance circuit (130) (see fig. 7).

Regarding claim 21, Roy teaches that the performance circuit includes a CMOS configuration (M3, M4) (see fig. 7).

Regarding claim 22, Roy teaches that the step of coupling includes coupling the protection circuit (102) to a p-channel device of the CMOS configuration (M3) (see fig. 7).

Regarding claim 23, Roy teaches that the step of forming a protection circuit includes forming a diode (102) and the step of coupling includes coupling the protection circuit (102) to a p-channel device of the CMOS configuration (M3) (see fig. 7).

Regarding claim 24, Roy teaches that the step of forming a protection circuit includes forming a unit diode (104), the unit diode comprised of a block of a doped region (P+) of the IC substrate (120) occupying an area of the substrate (P-well) sufficient to support a contact (VSS/INPUT) to the doped region (142, 144), a junction region (consider the junction formed between the P-well and the substrate 120) of the IC substrate surrounding the doped region (142, 144), and a contact (VSS/INPUT) to the doped region (142, 144) (see fig. 7).

Regarding claim 27, Roy teaches that the step of forming a performance circuit includes: forming a unit transistor device (M4) having a drain region (N+) comprised of a doped region of the a doped region (N+) of the IC substrate (120) occupying an area of the substrate sufficient to support a contact (VSS/OUTPUT) to the doped region; forming a gate region (M4) of the IC substrate surrounding the doped region; and forming a contact (VSS/OUTPUT) to the doped region (see fig. 7).

Regarding claim 28, Roy teaches that the doped region (N+) being a first doped region of a first dopant (N+) in a well (P-Well) of the substrate (120), the well being doped with a concentration of a second dopant (P) (see fig. 7) and wherein forming a performance circuit further comprises: forming a source region (N+) of the transistor doped with the first dopant (N+) in the well (P-Well) separated from the drain region (N+) by the gate to form a unit transistor (M4) (see fig. 7).

Regarding claim 29, Roy teaches forming a plurality of unit transistors (M3, M4) (see fig. 7).

Allowable Subject Matter

7. Claims 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach, disclose, or suggest, either alone or in combination, a unit diode as protection circuit comprising a doped region doped with a first dopant in the second well of the substrate, the second well being doped with a first concentration of a second dopant, and a junction region surrounding the first doped region and further separating the first doped region from the second well, wherein forming a protection circuit includes forming a third doped region in the second well adjacent the junction region, the third doped region doped with a second concentration of the second dopant.

Response to Arguments

9. Applicant's arguments with respect to claims 20-29 have been considered but are moot in view of the new ground(s) of rejection.

Correspondence

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800